

WHAT IS CLAIMED

1. A multiport switch comprising:

a plurality of receive ports, the receive ports receiving frames in a network, the frames having a source field indicating the source of the frame and a destination field indicating an intended destination for the frame;

5 a plurality of transmit ports, the transmit ports configured to transmit the frames in the network; and

a logic circuit coupled to the receive ports and configured to determine frame forwarding information for the received frames, the logic circuit including a plurality of address lookup tables, each of the address lookup tables including a plurality of addressable table entries for storing information relating to the frames, each of the addressable table entries including at least a port vector field that identifies ports corresponding to the frames of the addressable table entries and an address field that identifies network addresses of the frames, the logic circuit, when performing a write operation to one of the plurality of address lookup tables, determines the one of the 10 plurality of address tables to write to based on information in the received frame.

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2. The multiport switch of claim 1, wherein the logic circuit determines the one of the plurality of address tables based on the least significant bit of one of the source field and the destination field of the received frame.

3. The multiport switch of claim 1, wherein the plurality of receive and transmit ports are media access control (MAC) ports in an Ethernet network.

4. The multiport switch of claim 1, wherein the plurality of address lookup tables includes a first address lookup table and a second address lookup table, the logic circuit determining the address of the addressable table entries to write to based on a hash value generated using the network address of the frame.

5. The multiport switch of claim 4 wherein multiple entries written to the same address in the address tables are chained together serially.

6. The switch of claim 5, wherein the logic circuit includes a search circuit that searches for a desired address in the first and second address lookup tables based on the information in the received frame.

7. The multiport switch of claim 6, wherein the internal rules checking circuit determines the frame forwarding information based on the result of the search by the search circuit.

8. A method of using a lookup table implemented with a first lookup sub-table and a second lookup sub-table, the method comprising:
calculating a row address of the lookup table based on a hash value of a network address associated with an entry in the lookup table;
storing the entry in one of the first sub-table and the second sub-table at the calculated row address by writing the entry to the one of the first sub-table and the second sub-table based on the network address; and
accessing the entries stored in the lookup table by reading entries stored at a desired address in the first and second sub-tables.

9. The method of claim 8, wherein writing the entry to the one of the first sub-table and the second sub-table based on the network address further includes writing the entry to the one of the first and second sub-tables based on the least significant bit of one of a source field and a destination field of the network address.

10. The method of claim 8, wherein storing the entry further includes: creating a chain of entries beginning at the calculated row address when the calculated row address contains an entry.

11. The method of claim 10, wherein the chains of entries are implemented as a linked list.

12. The method of claim 10, wherein the first and second sub-tables are each partitioned into a bin portion and a heap portion, the bin portion storing a first entry in each of the chains of entries and the heap portion storing additional entries in each chain of entries.

13. The method of claim 8, wherein calculating the row address based on the hash value further includes:

concatenating the network address with a virtual local area network index to obtain a concatenated value; and

5 generating the hash value using a hashing function based on the concatenated value.

14. The method of claim 8, wherein accessing the entries includes reading a port vector field from one of the entries that matches a frame associated with the desired address.

15. The method of claim 14, further comprising generating a frame forwarding descriptor for the frame, the frame forwarding descriptor including information from the port vector field.

16. A multiport switch comprising:

a plurality of receive ports configured to receive frames, the frames including a source address and a destination address;

a plurality of transmit ports configured to transmit the frames to the respective

5 destination addresses;

first and second address tables, each of the first and second address tables including a plurality of addressable table entries, each addressable table entry storing frame forwarding information for one of the received frames; and

10 a logic device configured to calculate a first row address of the first and second

address tables that the frame forwarding information is to be stored at, determine

whether the frame forwarding information is to be stored in the first or the second

address table based on a pre-selected bit in the received frame, and store the frame

forwarding information in the determined first or second table in the first available entry

15 at the first row address as a table entry.

17. The multiport switch of claim 16, wherein the frames are data frames transmitted in an Ethernet network.

18. The multiport switch of claim 17, wherein the pre-selected bit is the least significant bit of one of a source address field and a destination address field of the data frame.
19. The multiport switch of claim 16, wherein the first row address is calculated based on hash value of the source or destination address of the data frame.
20. The multiport switch of claim 16, wherein storing the frame forwarding information in the determined address table includes storing multiple table entries in a link list structure, each of the multiple entries of each of the link list structures being in the same one of the first and second address tables and having the same calculated 5 row address.